The University of Texas at Tyler
Department of Electrical Engineering

Course: EENG 4331.060 – VLSI Design (Elective)

Syllabus

Catalog Description:

MOS transistor theory; CMOS manufacturing technology; Design and fabrication of digital integrated circuits; EDA tools for design of VLSI circuits; Physical Design Flow; Low Power IC Design; Design rules for VLSI Design; CMOS Logic Design; datapath circuits and subsystem design issues; Testing and verification of Integrated circuits. Three hours of lecture each week.

Prerequisites: EENG 3302 Digital Systems, EENG 3306 Electronic Circuit Analysis I

Credits: (**3** hours lecture, **0** hours laboratory per week)

Text(s): N. H. E. Weste and D. Harris. *CMOS VLSI Design.* 4th Edition. Pearson-Addison-Wesley, 2011. ISBN 978-0321-547743

Additional Material(s): Class Notes; Journal Articles; Online Certification

Course Coordinator: Prabha Sundaravadivel, Assistant Professor, Electrical Engineering

Topics Covered: (Paragraph of topics separated by semicolons)

VLSI CAD Tools; Fabrication of Integrated Circuits; Modeling Submicron Transistors; Static and Dynamic Logic Gate Design; Datapath design; Subsystem design; Delay, Power Characterization; Clock Distribution; Physical Design; Interconnect Modelling; Testing and Verification Issues.

Evaluation Methods (Only items in dark print apply):

1. Examinations/ Quizzes
2. Homework
3. Report
4. Computer Programming
5. Project
6. Presentation
7. Course Participation
8. Peer Review

Course Objectives[1]: By the end of this course students will be able to:

[1] Numbers in brackets refer to method(s) to evaluate the course objective

1. Describe the processing steps for creating a CMOS Integrated Circuit. [1,2]
2. Analyze different operating regions for MOSFET through current equations. [1,2]
3. Model digital circuits using Register-to-Transfer Logic (RTL) programming. [4,5]
4. Design a static CMOS Logic gate. [1]
5. Analyze different nanoscale devices. [1]

6. Optimize the device sizing for a complex logic circuit using the concept of logical effort. [1,2]
7. Determine the delay in CMOS circuits. [1]
8. Characterize a CMOS logic gate utilizing SPICE simulation data. [4,5]
9. Implement transistor-level schematic of compound CMOS logic gates. [2]
10. Assess the design challenges of implementing dynamic logic circuits in submicron technologies. [1]
11. Analyze different memory architectures in the transistor-level. [1,2]
12. Identify the issues with testing complex logic circuits. [1,2]
13. Understand the issues with designing devices and circuits using nanotechnology. [1]
14. Describe the steps involved in physical design flow. [1,7]
15. Explore the current research trend in VLSI Design. [6]

Relationship to Program Outcomes (only items in dark print apply)[2]. This course supports the following Electrical Engineering Program Outcomes, which state that our students will:

[2] Numbers in brackets refer to course objective(s) that address the Program Outcome.

1. Have the ability to apply knowledge of the fundamentals of mathematics, science, and engineering; [1,2]
2. Have the ability to use modern engineering tools and techniques in the practice of electrical engineering; [3,8]
3. Have the ability to analyze electrical circuits, devices, and systems; [9,10]
4. Have the ability to design electrical circuits, devices, and systems to meet application requirements; [4,11]
5. Have the ability to design and conduct experiments, and analyze and interpret experimental results;
6. Have the ability to identify, formulate, and solve problems in the practice of electrical engineering using appropriate theoretical and experimental methods; [6,12,]
7. Have effective written, visual, and oral communication skills; [15]
8. Possess an educational background to understand the global context in which engineering is practiced, including:
   a. Knowledge of contemporary issues related to science and engineering; [14]
   b. The impact of engineering on society;
   c. The role of ethics in the practice of engineering;
9. Have the ability to contribute effectively as members of multi-disciplinary engineering teams;
10. Have a recognition of the need for and ability to pursue continued learning throughout their professional careers; [13]

Contribution to Meeting Professional Component: (in semester hours)

Mathematics and Basic Sciences:	0	hours
Engineering Sciences and Design:	3	hours
General Education Component:	0	hours

Prepared By: Prabha Sundaravadivel

Date: 22-Aug-2018

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COURSE OUTLINE

Course Coordinator:

Dr. Prabha Sundaravadivel,
Assistant Professor, Department of Electrical Engineering
Office: RBN 1008
Email: PSundaravadivel@uttyler.edu
Office Hours: Tue/Thur 10:45 AM – 12:15 PM
Email and Discussion Boards.

Class Location/Time: Online Lectures

Grading Policy:

Homework	15% (6% + 3% + 3% + 3%)	No. of HomeWorks - 4
Participation	10%	Engagement through Discussion Boards and email
Labs/ Mini Projects	20%	No. of. Assignments – 4
Reading Assignments	15%	Total of 3 components: 1. Online course 2. 2 Research Papers
Mid Term Exam	15%	
Final Exam	25%	
Total	**100%**	

Semester Schedule:

Week	Date	Topics	Homework	Lab/ Mini Project
1	Aug 27	Course Overview, Introduction to VLSI CMOS Logic Gates		
2	Sept 4	CMOS Manufacturing, MOS Transistor Theory	Hw1	
3	Sept 10	MOSFET I-V and C-V Characteristics,	Hw1 due	
4	Sept 17	CMOS Design issues, Introduction to Verilog and EDAs	Hw2	Lab 1

5	Sept 24	Power Estimation, Interconnect Modeling	HW-2 due	
6	Oct 1	Low Power Design, Delay Characterization		Lab 1 due
7	Oct 8	Mid Term		Research Paper 1,2
8	Oct 15	Combinational Circuit Design, Static and Dynamic Logic Circuit Families		Lab 2
9	Oct 22	Sequential Circuit Design	Hw3	Lab 2 due
10	Oct 29	Datapath Subsystem	Hw3 due	Lab 3
11	Nov 5	Memory Design	Hw4	Lab 3 due
12	Nov 12	Design for Testing, Verification	Hw4 due	
13	Nov 19	Thanksgiving Week		
14	Nov 26	Research Paper (1,2) Review	Online course Certificate due	Lab 4
15	Dec 3	Review and Future Directions		Lab 4 due
16	Dec 10	Final Exam		

Homework:

There will be a total of 4 assignments. Homework 1,3 and 4 will be in the form of problems and theory questions. Homework-2 will be a take home quiz to test the understanding of basic concepts. Homework will be assigned by Monday as per the schedule and will be due on Friday of the following week. No late homework will be accepted. Homework problems/ questions may be discussed with other students, but the final submission should be an original and independent solution.

Lab/Mini Project:

Four labs or mini projects will be assigned throughout the semester. The topics to be covered here are: Verilog programming and Circuit design. The following software are to be used for the lab assignments:

1. ModelSim Student Edition - https://www.mentor.com/company/higher_ed/modelsim-student-edition
2. LTSpice - http://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html

Online Certification:

Physical Design Flow is an advance topic in VLSI, the knowledge of which would help in securing jobs in VLSI industry. The instructor for this recommended online course is from the VLSI Industry. This course is added as a part of reading assignment with 5% weightage. The discounted cost of this course is around $10 and the total duration of lectures in 5 hours. If the course is not

available at the discounted price, email the Instructor. This self-paced course needs to be completed by Week 14 to earn course credit for the same. Here is the link for the course:

https://www.udemy.com/vlsi-academy-physical-design-flow/

Research Reading Assignments:

Two research papers will be assigned by the Mid-Term week. Students are expected to read them and make a 10-minute presentation for each paper. This presentation can be done either through zoom meeting or a recorded presentation. The total of 20-minute presentation will have 10% weightage.

Exam:

This course will have MidTerm and Final exam. The MidTerm exam will have 15% weightage and Final exam will have a 25% weightage. In addition to this, there will be a take home quiz (6% weightage) which will be assigned during week 4.

Academic Integrity:

Students should be aware that absolute academic integrity is expected of every student in all undertakings at the University of Texas at Tyler. A plagiarism check will be done all the reports submitted by students. Copied or unoriginal solutions will result in a "0" in that course component. An evidence of a pattern in academic dishonesty will lead to strong university-imposed penalties.

Participation:

Since this is an online course, to stay more engaged in the subject, participation in the discussion boards are expected. Based on the degree of participation in 5 such discussions, the grades will be awarded for a total of 10% (2% each).

Accommodation:

If you have a disability, including a learning disability, for which you request disability support services/accommodation(s), please contact the Disability Support Services office, so that the appropriate arrangements may be made. In accordance with the Federal Law, a student requesting disability support services/accommodation(s) must provide appropriate documentation of his/her disability to the Disability Support Services Counselor. For more information, call or visit the Student Accessibility and Resources Center located in the University Center, Room 3150. The Telephone number is 903.566.7079. Additional information may also be obtained at the following UT Tyler website: https://www.uttyler.edu/disabilityservices/

Happy Learning!