The University of Texas at Tyler
Department of Electrical Engineering

Course: EENG 5335 – FPGA Design

Syllabus

Catalog Description:

Digital Systems design with Field Programmable Gate Arrays (FPGAs); Design and synthesis of reconfigurable logic with High-level Hardware Description Language; Logic Design using FPGAs; Architectural and System Design issues; Reconfigurable computing with FPGAs. Three hours of lecture each week.

Prerequisites: EENG 3307 Microprocessors and EENG 4309 Electronic Circuits II or Consent of Instructor

Credits: (**3** hours lecture, **0** hours laboratory per week)

Text(s): N. H. E. Weste and D. Harris. *Fundamentals of Digital Logic with VHDL Design.* 3rd Edition. Mc Graw Hill, 2008. ISBN 978-0077221430

Additional Material(s): Peter J. Ashenden, The Student's Guide to VHDL. 2nd edition. Morgan Kaufmann, 2008.

Class Notes; Journal Articles

Course Coordinator: Prabha Sundaravadivel, Assistant Professor, Electrical Engineering

Topics Covered:
(Paragraph of topics separated by semicolons)

VLSI CAD Tools; Fabrication of Integrated Circuits; Modeling Submicron Transistors; Static and Dynamic Logic Gate Design; Datapath design; Subsystem design; Delay, Power Characterization; Clock Distribution; Physical Design; Interconnect Modelling; Testing and Verification Issues.

Evaluation Methods (Only items in dark print apply):

1. Examinations/ Quizzes
2. Homework
3. Report
4. Computer Programming
5. Project
6. Presentation
7. Course Participation
8. Peer Review

Course Objectives[1]: By the end of this course students will be able to:

1. Explain how FPGAs are used in digital system design. [1,2]
2. Design digital logic circuits using VHDL. [1,2]
3. Use CAD tools in the design, simulation, and implementation of FPGA designs. [4,5]

4. Analyze the implementation of reconfigurable logics in FPGA design process [1]
5. Design and implement Combinational and sequential logic circuits with FPGAs. [1,2,7]
6. Design and implement Finite State Machines using HDL [1,2,4]
7. Identify the issues at the architectural level associated with reconfigurable logic. [1,7]
8. Explore the real-time advance applications of FPGA boards. [3,6]
9. Explore the current research trend in FPGA Design. [6]
10. Describe the steps involved in physical design flow. [1,7]
11. Explore the current research trend in VLSI Design. [6]

[1] Numbers in brackets refer to method(s) to evaluate the course objective

Relationship to Program Outcomes (only items in dark print apply)[2]. This course supports the following Electrical Engineering Program Outcomes, which state that our students will:

1. Breadth and Depth: Students will be able to apply knowledge at a graduate level in two of the following areas: electronics, power systems, controls, advanced engineering mathematics, signal processing. [1,2,13,14]
2. Modern Engineering Tools: Students will be able to use modern engineering tools for analysis and design as applied to engineering problems. [3,8]
3. Advanced Engineering Mathematics: Students will be able to apply principles of advanced engineering mathematics including probability and statistics to engineering problems. [9,10]
4. Systems Design: Students will be able to apply systems design approaches including modeling and simulation of interacting sub-systems to complex engineering problems. [4,11]
5. Design Methods: Students will be able to demonstrate application of design methodology by comparing and evaluating solutions to engineering problems. [6,12]
6. Communication Skills: Students will demonstrate effective oral, visual and written communication skills from a technical perspective. [15]

[2] Numbers in brackets refer to course objective(s) that address the Program Outcome.

Contribution to Meeting Professional Component: (in semester hours)

Mathematics and Basic Sciences:	0	hours
Engineering Sciences and Design:	3	hours
General Education Component:	0	hours

Prepared By: Prabha Sundaravadivel

Date: 22-Aug-2018

The University of Texas at Tyler
Department of Electrical Engineering

Course: EENG 5335.001, 040 – FPGA Design

COURSE OUTLINE

Course Coordinator:

Dr. Prabha Sundaravadivel,

Assistant Professor, Department of Electrical Engineering
Office: RBN 1008

Email: PSundaravadivel@uttyler.edu

Office Hours: Thur 11 AM – 12:30 PM, 2:30 PM – 4:00 PM

Class Location/Time: EENG 4332.001 – RBN 02012,

EENG 4332.040 – Houston Engineering Center 0A216

Grading Policy:

Participation	15%	Attendance (5%), occasional short assignments (FSM) or quiz, and engagement through discussions.
Project	35%	
Reading Assignments	10%	2 Research Papers
Exams	40%	2 Exams
Total	**100%**	

Semester Schedule (tentative):

Week	Date	Topics
1	Jan 17	Course Overview, Introduction to FPGA and system level implementation
2	Jan 24	Introduction to logic circuits and FPGA architecture
3	Jan 31	Introduction to Verilog and VHDL
4	Feb 7	Number Representation and Combinational circuit
5	Feb 14	Combinational Circuit
6	Feb 21	Sequential Circuit
7	Feb 28	Exam 1
8	Mar 7	Sequential Circuit
9	Mar 14	Spring Break
10	Mar 21	Synchronous Sequential Circuits
11	Mar 28	Synchronous Sequential Circuits
12	Apr 4	Synchronous Sequential Circuits
13	Apr 11	Exam 2
14	Apr 18	Research Paper 1,2 Review

15	Apr 25	Research Paper 1,2 Review
16	May 2	Finals week - Project presentation

Short Assignment and Quiz:

There will be about 3-4 short assignments or quiz, after significant topics such as Finite State Machines, is discussed in the class. The purpose of this is to help in assessing the understanding of topics. About a week's time would be given for each assignment submission and quiz preparation. This will account for 10% of grade. No late submissions will be accepted. Assignment problems/ questions may be discussed with other students, but the final submission should be an original and independent solution.

Project:

Project will be based on Basys 3 FPGA boards. Students can either form a group of 2-3 or do the projects individually. Students can choose the topic for the project either from the given topics or choose their own. Project topics will be given by Jan 31, 2019. The tentative schedule for project completion is:

Abstract submission (5%) due – Feb 21, 2019

Mid Term Report (10%) due – March 21, 2019

Final Report (10%) due – April 30, 2019

Project Presentation (10%) due – May 2, 2019

Research Reading Assignments:

Two research papers will be assigned before the Mid-Term week. Students are expected to read them and make a 10-minute presentation for each paper. This presentation will be reviewed on last 2 weeks of the course. The total of 20-minute presentation will have 10% weightage.

Exam:

This course will have 2 exams with 20% weightage for each. There is no Final Exam for this course.

Academic Integrity:

Students should be aware that absolute academic integrity is expected of every student in all undertakings at the University of Texas at Tyler. A plagiarism check will be done all the reports submitted by students. Copied or unoriginal solutions will result in a "0" in that course component. An evidence of a pattern in academic dishonesty will lead to strong university-imposed penalties.

Attendance:

As an emphasis on consistent participation of students throughout the course, attendance will be taken after each class lecture.

Accommodation:

If you have a disability, including a learning disability, for which you request disability support services/accommodation(s), please contact the Disability Support Services office, so that the appropriate arrangements may be made. In accordance with the Federal Law, a student requesting disability support services/accommodation(s) must provide appropriate documentation of his/her disability to the Disability Support Services Counselor. For more information, call or visit the Student Accessibility and Resources Center located in the University Center, Room 3150. The Telephone number is 903.566.7079. Additional information may also be obtained at the following UT Tyler website: https://www.uttyler.edu/disabilityservices/

Happy Learning!